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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
WHITE, DYLAN C

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,712	DROTTAR ET AL.	
	Examiner	Art Unit	
	Dylan White	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 7/10/2006. These drawings are accepted as replacement sheets.

Specification

The correction to the specification received on 7/10/2006, to fix minor informalities in the specification has been entered.

Response to Arguments

Applicant's arguments filed an 7/10/2006 have been fully considered but they are not persuasive. Regarding a second circuit input port coupled to an output port of the first circuit. The Voshell reference clearly anticipates the output of a first circuit coupled to the input of a second circuit.

In response to Applicant argument that Arcoleo's description of physical characteristics of transistors does not disclosed the claimed subject matter. The size of each transistor is determined by its physical characteristics (length, width, capacitance, and channel resistance), therefore the transistors can be sized in which ever way the user desires.

In regards to Applicants assertion to prima facie cause of obviousness with respect to claims 4-5 and 7-10 the Applicant is incorrect in the arguments with respect to motivation and undesirable combination.

First, Applicant believes the initial Office Action failed to point out in either prior art disclosure a motivation to combine the references. However, motivation of signal quality and impedance matching purposes were clearly stated in the first Office Action. It can be seen, even the abstract of Arcoleo, that the selectable output drive strength buffer can be "closely tailored to the electrical load being driven (impedance matching), signal reflections, voltage overshoot and undershoot, and timing problems that can all result from mis-match between the output buffer drive strength and the associated electrical load". Matching the impedance of the load reduces the signal reflections, voltages over/under, and timing problems as stated above and improves the signal quality, therefore proper support for the prima facie case of obviousness had been established without the use of improper hindsight.

Second, Applicant argues that the combination of Voshell and Arcoleo would be undesirable, but Applicant has used piecemeal analysis of the prior art to construct an argument.

When looking at the Arcoleo quote the Applicant used;

> **While output buffers having selectable drive strength have previously been used with other devices, such as programmable logic devices**, selectable drive strength output buffers that allow a user to adjust the output buffer drive strength have not heretofore been used with semiconductor memory devices. There are several reasons for this.

Applicant states that Arcoleo discourages the use of selectable drive strength buffers with programmable logic devices, but the quote the applicant has provided clearly explains that the use of a selectable drive strength buffer together used with programmable logic devices is well known in the art and has been done before. This is exactly why the Examiner cited the reference in the initial rejection of the claims and therefore is not undesirable.

Furthermore, Arcoleo states here that selectable drive strength buffers have not been previously used in semiconductor memory devices as the inventor Arcoleo is applying his selectable output drive strength buffer to a memory chip. The several reasons for this combination with a memory chip (which have no bearing in regards to the present application) are disclosed in col. 3, lines 12-26.

Regarding arguments to claims 20-22, the Applicant disclose a failure of prima facie cause of obviousness and impermissible hindsight to reject claimed subject matter as there is question if Martin requires any impedance matching. The prior art reference of Martin et al. (US 6,894,536) discloses a voltage driver (12 @ Fig. 8) for a transmission line, where only a single driver (76/78) is used for each transmission line respectively. Therefore there is no impedance matching being done with the voltage driver of Martin, but if a variable strength output driver used it would allow for increased impedance matching between the transmitter and receiver. Impermissible hindsight was not used.

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, are rejected under 35 U.S.C. 102(e) as being anticipated by Martin et al. (US 6,704,818).

Regarding claim 1, Martin discloses a first circuit (8 - comprising 8a, 8b, 8c) coupled to an input port (4) of the transmitter (2); and a second circuit (comprising 8b, 8b, 8b) including a second circuit input port (between 8c and 8b, not shown) coupled to an output port (of 8c, not shown) of the first circuit (8 - comprising 8a, 8b, 8c), the second circuit includes a second circuit output port (16) coupled to an output port of the transmitter (6), where the fist circuit is sized with respect to the second circuit (col. 3, lines 19-35) such that for a pulse signal applied to the input port (4), the transmitter (2) generates an output signal having a rise-time and fall-time that are substantially equal at the output port (Fig. 3).

Regarding claim 2, Martin discloses where the first circuit (8 - comprising 8a, 8b, 8c) includes an inverter (8a).

Regarding claim 3, Martin discloses where the inverter (8a) includes a N-type MOSFET (26) connected in series with a P-type MOSFET (24).

Regarding claim 6, Martin discloses where the second circuit (8b) discloses a plurality of driver circuits (Fig. 4).

Regarding claim 7, Martin discloses where each of the plurality of driver circuits (Fig. 4) includes a P-type MOSFET transistor (24, 28, 32, 36, 40, 44) connected in series with an N-type MOSFET (26, 30, 34, 38, 42, 46).

Regarding claim 8, Martin discloses where P-type MOSFET is sized to source a first current (from V_{cc} 20) and the N-type MOSFET is sized to sink a second current (to GND 22) substantially equal to the first current (the transistors have to be sized in order to handle the substantially equal first and second currents. If the transistors were too small they would burn out).

Regarding claim 9, Martin discloses where the second circuit (comprising 8b, 8b, 8b) is connected to an equalization control circuit (18).

Regarding claim 10, Martin discloses where the equalization control circuit provides de-emphases (col. 3, lines20-23).

Regarding claim 11, Martin discloses where the transmitter transmits at a signal level (1/2 swing, Fig. 3) and the first circuit and the second circuit are coupled to a supply potential having a value of about twice the signal level (V_{cc}).

Regarding claim 12, Martin discloses receiving a signal (4) at a first circuit (8 - comprising 8a, 8b, 8c); in a second circuit (comprising 8b, 8b, 8b) coupled to the first circuit (output of 8c coupled to input of 8b @ Fig. 4) the second circuit including a plurality of P-type MOSFETs (24, 28, 32, 36, 40, 44), enabling the plurality of P-type MOSFETs to drive a transmission line (col. 4, lines 30-33); and enabling less than the plurality of P-type MOSFETs to drive the transmission line (col. 3, lines 23-31), where the fist circuit is sized with respect to the second circuit (col. 3, lines 19-35) such that for a pulse signal applied to the input port (4), the transmitter (2) generates an output signal having a rise-time and fall-time that are substantially equal at the output port (Fig. 3).

Regarding claim 13, Martin discloses where receiving a signal at a first circuit includes receiving a digital signal (@ input 4).

Regarding claim 14, Martin discloses where enabling the plurality of P-type MOSFETs to drive a transmission line includes enabling the plurality of P-type MOSFETS substantially simultaneously (72, 74, 76, 78 @ Fig. 5).

Regarding claim 15, Martin discloses where enabling less than all of the P-type MOSFETs to drive the transmission line comprises enabling less than all of the P-type MOSFETs substantially simultaneously (72 @ Fig. 5; col. 3, lines 61-65).

Regarding claim 16, Martin discloses a transmitter (2) including; a first circuit (8 – comprising 8a, 8b, 8c) coupled to an input port of the transmitter (4); and a second circuit (comprising 8b, 8b, 8b) coupled to the first circuit (output of 8c to input of 8b) to an output port (16) of the transmitter (2), the second circuit coupled to an equalization circuit (18) wherein the equalization circuit provides de-emphasis (col. 2, lines 58-62); a receiver (col. 1 & 2, lines 66-67 & 1-2); and a transmission (col. 4, lines 30-33), lines line to couple the output port (16) of the transmitter (2) to the receiver.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-5, and 7- rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (US 6,704,818) in view of Arcoleo et al. (US 5,864,506).

Regarding claim 4, Martin discloses the output driver of claim 3, but fails to teach the N-type MOSFET being larger than the P-type MOSFET.

Arcoleo discloses an output driver having selectable strength, where the first circuit is an inverter comprising a PMOS (603a) and an NMOS (603b) connected in series (603), where the N-type MOSFET is larger than the P-type MOSFET (col. 8, lines 20-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use the driver/transmitter circuit of Martin with the transistor sizing taught by Arcoleo for impedance matching and improved signal quality.

Regarding claim 5, the combination teaches the where the N-type MOSFET is between about two and about three times larger than the P-type MOSFET (Arcoleo col. 8, lines 20-26). Furthermore the MPEP states (2144.04 IV. A)

> In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Therefore, simply changing the size of the transistors does not change the operation of the circuit to give it any patentable weight over the prior art.

Regarding claim 17, the combination discloses where the first circuit (8 - comprising 8a, 8b, 8c) including an inverter (8a) having a P-type MOSFET and an N-type MOSFET (Fig. 4), the N-type MOSFET being between about two and about three times larger than the p-type MOSFET (Arcoleo col. 8, lines 20-26).

Regarding claim 18, the combination discloses where the second circuit (8b, 8b, 8b) includes a voltage driver (Martin, col. 2, lines 14-15).

Regarding claim 19, the combination discloses where the second circuit includes a controllable source impedance (Arcoleo, 606a, 607a @ Fig. 6).

Claims 20-23, are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al. (US 6,704,818) herein after (Martin-818) in view of Martin et al. (US 6,894,536) herein after (Martin-536).

Regarding claim 20, Martin-818 discloses a first circuit (8 – comprising 8a, 8b, 8c) coupled to an input port (4) of the transmitter (2)l and a second circuit (8b, 8b, 8b) including a second input port (between 8c and 8b, not shown) coupled to an output port of the transmitter (16), where the fist circuit is sized with respect to the second circuit (col. 3, lines 19-35) such that for a pulse signal applied to the input port (4), the transmitter (2) generates an output signal having a rise-time and fall-time that are substantially equal at the output port (Fig. 3). Martin-818 fails to disclose a first processor including a transmitter and a second processor including a receiver.

Martin-536 discloses a first processor (60) including a transmitter (12) and a second processor (62, col. 5, lines 29) including a receiver (16) coupled to the transmitter (12) through a transmission line (14), therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use the driver/transmitter of Martin-818 and the processor communication line taught by Martin-536 for impedance matching between transmitter and receiver.

Regarding claim 21, the combination discloses where the first processor includes a very long instruction word processor (Martin-536, col. 5, lines 23-29).

Regarding claim 22, the combination discloses where the second processor includes a complex instruction set processor (Martin-536, col. 5, lines 23-29).

Regarding claim 23, the combination comprises an equalization control circuit (Martin-818, 18 @ Fig. 4) coupled to the second circuit (8b, 8b, 8b) to provide de-emphasis (col. 2, lines 58-62).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dylan White whose telephone number is (571) 272-1406. The examiner can normally be reached on m-f 7:30- 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dylan White
Patent Examiner, AU 2819

REXFORD BARNIE
SUPERVISORY PATENT EXAMINER